CRAIG B. WATSON
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SUMMARY:

Electrical Engineer with a strong background in embedded applications, communications, real-time programming, and firmware development.

EDUCATION and CERTIFICATIONS:

Wind River Linux Development training.
Xilinx FPGA training (Verilog).
Xilinx FPGA training (VHDL).
Comprehensive VHDL Mentor Graphics training course.
Airborne Radar I & II, Brevard Community College.
M.S.T.M. Embry-Riddle Aeronautical University.
B.S.E. Electrical Engineering, University of Central Florida.
Clearances: Top Secret/SBI July 1989, Secret November 1997, Top Secret October 2005.

TECHNICAL SYNOPSIS:

Programming Languages:

High level:
Basic
C/C++
FORTRAN
HTML/XHTML
Java
Server Side CGI
Perl / PHP / Lua / Java Script
PL/M
UML
Verilog
VHDL

Assembly (microprocessors):
Arm Cortex M3, A8
Intel 8085, 8051, and 80x86
Microchip PIC32, PIC24
MIPs 74kc
Motorola 6805, 68HC11, 68040, and 88100 RISC
NEC 7500 and 7556
Power PC 440, 6xx, 74xx
Reneasas H8
Zilog Z8

Operating Systems:

Linux	LynxOS	Mercury OS	MS-DOS
Open VMS	OS-X	pSOS	Solaris
UNIX	Virtuoso	VxWorks	Windows

Hardware:

Digital Design	Telephone Interface	Intrinsic Safety
Storage Applications	Networking, WIFI	Low Power Applications
FPGA HDL Development	USB, SATA, Fibre Channel, SCSI Interfaces	

EXPERIENCE:

Vanguard Ruggedized Storage

Part-time Consulting, March 2013 – July 2017

Hardware and Software design and engineering services for rugged storage products.
Duties and Activities:

- Marketing and product strategy.
- Work on new product proposals.
- Meet with representation firms handling technical aspects of business.
- Lead architecture design and development.
- Software and Hardware design, development and debugging.
- Support of various products.

Tasks and Accomplishments:

- Provide demo and support for a proposal effort to put a recording device on a F-15.
- Design of VPX hardware interface for a storage device.
- Developed prototype COM Express based Fibre Channel data storage subsystem for a high altitude reconnaissance aircraft. Achieved data rates of >340 MB/s writing and >640 MB/s reading. Some throughput tools developed in C++.
- Worked with Linux LIO kernel developers to troubleshoot and fix Fibre Channel issues with customer equipment.
- Developed ruggedized Fibre Channel storage subsystem based upon above prototype.
- Implemented new Data Destruction feature into product.

Data Flow Systems

Contract Programming, June 2016 – August 2016

Linux kernel programming for an ARM-based SCADA radio communications and control device.
Tasks and Accomplishments:

- Developed Linux touchscreen device driver and device tree overlay for ARM A8 platform.
- Revamp Linux cross-compile build system.
- Set up Git repository for product code.
- Assist with new hardware startup.

Reliable Systems Services

Senior Software Engineer, August 2013 – February 2016

Programming embedded processors in smart encrypted radio WAN L2 bridge applications.
Tasks and Accomplishments:

- Set up cross-compile development process for new Qualcomm/Altheros MIPs based modem product using “git” for configuration management.
- Developed Java application demonstrating querying products using SNMP to display and log system performance parameters.
- Wrote Linux platform startup code for new product.
- Back-ported / wrote Ethernet PHY device driver and integrated into new product. Fixed MAC layer problems in Qualcomm/Atheros code.
- Ported high speed serial UART driver to new platform and integrated into new product.
- Assisted in bringing up new hardware.
- Wrote Perl scripts used to benchmark networking performance with Candela application.
- Ported openssl and lighttpd packages to new product.
- Developed new cgi-based web interface for new product.
- Ported several proprietary protocol drivers from PPC kernel 2.6.20 to MIPS kernel 3.3.8.
- Implemented a simplified state machine for protocol removing entangled modes. This rewrite addressed several race conditions and unexpected events in previous implementation provided by a subcontractor.
- Added a mode to state machine to support a sector antenna controller.

Reliable Systems Services

Senior Software Engineer, January 2013 – February 2013

Tasks and Accomplishments:

- Programmed Embedded Power PC processor in a smart encrypted radio WAN router.
- Set up a new cross-compilation development workstation (ELDK SDK for PPC).
- Re-engineered Subversion-based PPC build process to track configuration changes.

Position terminated due to sequestration schedule changes.

DRS Technologies

Senior Software Engineer, February 2012 – August 2012

Programmed PIC and H8 embedded System Management Controllers supporting Intel i7s. Real-time work performed using UML code generation of C++ with object oriented architecture.
Tasks and Accomplishments:

- Reviewed and edited several System Requirements Specifications and Unit Test Plans.
- Fixed USB HID/CDC composite interface.
- Identified several hardware design deficiencies and assisted in proper configuration of complex audio chain.
- Benchmarked the systems to determine best performance options for BIOS parameters. Benchmarks in C and C++ using Intel and Microsoft Visual C++ compilers.
- Investigated adding PECI support and DPTF to the systems.
- Assigned to back port Video for Linux driver from Red Hat Enterprise Linux 6.0 to 5.6.

Metsys LLC

Contract Programming DRS BAA, August 2011 – November 2011

Contract programming for DRS Technologies for a prototype handheld Android Accessory communication device. Real-time embedded programming performed in C for a Microchip PIC 32-bit microcontroller.
Tasks and Accomplishments:

- Developed user hardware interface.
- Developed Android Accessory USB interface.
- Developed File System, and TCP/IP communications.
- Assisted initial startup and debugging of new hardware.

Vanguard Ruggedized Storage

Vice President of Research and Development, March 2008 – June 2011
Part-time Consulting, November 2011 – February 2012

Responsible for product architecture and software development for storage product line. These ranged from a 14 TB ruggedized system to a 3-module 320GB device used to read logging modules collected from field systems. Programming performed in C, HTML, and server side CGI scripting in an embedded Linux environment. Programming in Verilog and C for Xilinx Virtex 5 FPGAs.
Duties included:

- Marketing and product strategy.
- Project planning and scheduling.
- Project engineering and development.

Activities included:

- Meeting with customers and vendors.
- Leading architecture design and development teams.
- Software development.
- Hardware design and debugging.
- Leading development of USB to SATA bridge device based on Xilinx Virtex 5 FPGAs.
- Leading development of 3 Network Attached Storage (NAS) devices.
- Provided support for other storage devices including PMC/PCI and SCSI RAID devices.

Tasks and accomplishments:

- Lead local sales and engineering office in Melbourne.
- Implemented a software configuration management system (Subversion).
- Developed company software procedures and standards.

- Developed user interface for new Network Attached Storage (NAS) product line.
- Implemented SNMP agent for above NAS devices.
- Wrote software specifications for outside contractors.
- Wrote Manufacturing Procedures for new products.
- Wrote Operations Manuals for new products.

Northrop Grumman Corporation

Various Programs

Senior Software Development Engineer, November 1997 – March 2008

RAMICS Program December 2007 – March 2008

Developed a high speed data recorder and injector (playback) for data being produced at 60 MB/s per channel on fiber optic Serial Front Panel Data Port (SFPDP) lines. RAMICS is a Navy program consisting of a LIDAR controlled weapon system on a helicopter for clearing mines in shallow water. Real time code developed in C for an embedded Linux system with user interface control code developed in C++ compiling for Windows and Linux using the QT libraries.

AIMS Program December 2007 – March 2008

Development of a 2-channel high speed RADAR video recorder for data being produced on Gigabit Ethernet. This was targeted for the Air Force Global Hawk program interfacing with the MP-RTIP sensor. This worked in conjunction with the AIMS data publishing, subscribing, and querying architecture. Real-time code on Linux platforms developed in C. Control code on Windows platform in C++.

COBRA Program July 2007 – January 2008

Selected to fix a high speed data recording application for the Navy's COBRA program. COBRA is an airborne multi-spectral mine detection system. This involved working with several sub-contractors at the device driver and system/application level. Work included kernel/device driver programming on an embedded Linux RAID system with a SCSI interface and application level programming with Windows XP. Data rates of 196 MB/s were realized on the Linux RAID device and an overall sustained system throughput of greater than 70 MB/s was achieved by the application.

ALMDS LRIP Program August 2006 – July 2007

Developed a 4-channel high speed recorder and injector (playback) for data being produced at 100 MB/s per channel on fiber optic Serial Front Panel Data Port (SFPDP) lines. Real time code was developed in C for an embedded Linux system with user interface control code developed in C++ compiling for Windows and Linux using the QT libraries. Control interface included a near real-time display of video data during flight. I flew as mission support specialist on Navy aircraft (SH60) during testing. Recorders functioned flawlessly during flight tests recording several terabytes of data. Injectors used extensively in support of primary application development.

ALMDS LRIP Program Software IPT Lead, September 2005 – August 2006

Led a team rehosting the ALMDS APS for the Low Rate Initial Production (LRIP) upgrade. The ALMDS LRIP APS consists of a large Class IV laser and 4 cameras with 10 Power PC (PPC) CPUs and 10 Virtex IV Pro FPGAs for the image recognition/data processing. All processing is done in a real-time environment with VxWorks. Duties included estimation and development of software portion of bidding process for the LRIP program. This program was nominated to Aviation Week and Space Technology Magazine's Program of the Year. It was also nominated to EE Times 2006 Ace Awards Design Team of the Year competition.

ALMDS EMD Program Software Team Lead, February 2004 – September 2005

Led software team in implementation and development of embedded DSP and control software for the Airborne Laser Mine Detection System (ALMDS) APS. This consists of Sharc-based DSP parallel processing running in a Wind River Virtuoso real-time environment performing digital laser image processing. The ALMDS EMD APS consists of a large Class IV laser and 4 cameras with 48 Sharc CPUs for the data processor. All processing is done in a real-time environment. 67% of existing code base (35,000 lines) was modified. Only 202 lines of code were modified in 5 ½ months of flight testing. Flight testing was successful and Northrop Grumman secured the contract for low rate initial production (LRIP).

CWIN Videoswitch May 2003 – February 2004

Led software development for an embedded control application integrating a Crestron video controller and Extron 64x64 video switch matrix with a local area network interface application and several high definition frame grabbers. Programming accomplished with Microsoft Visual Studio.

JCP Program January 2003 – May 2003

Led software development for Navy Joint Stars Connectivity Package. This program exploits Joint Stars satellite data using an ARC/231 Satcom radio and a Sun workstation. Tasks included identifying an appropriate synchronous serial interface, porting/writing a serial device driver for a Digi Sync 570i synchronous interface card, porting a MIL STD 188-184 DAMA Link Layer protocol library, and porting proprietary application layer communications software to a Sun Workstation.

ALMDS Program September 2002 – January 2003

Completed implementation of a high speed data recorder and developed a real-time injector (playback) for the Airborne Laser Mine Detection System. The recorder and injector platforms were on a Mercury Vantage Race++ PCI system with a SCSI mass storage array connected via a proprietary fiber optic link to the Laser pod. The fiber optic link used a reconfigurable field gate array (FPGA) as an interface. The success of this work was a direct result of my involvement in the Northrop Grumman HPC IR&D program.

HPC Program November 2001 – January 2003

Led the Northrop Grumman High Performance Computing IR&D program. This involved development of portable parallel processing algorithms for image recognition using MPI. Three platforms -- CSPI BOS (w/Myrinet communications), Mercury Race++, and Linux Beowulf (PPC G4) -- clusters were used. In addition, a major effort was made to assess various FPGA development technologies for reconfigurable computing applications. This concentrated on using reconfigurable FPGA-based fiber optic I/O cards for high speed data transfer and preliminary digital signal processing. This technology fed the parallel processing algorithms.

SATCOM Program February 2000 – November 2002

Developed architecture and system software for Joint Stars SATCOM satellite communications enhancement program. This involved implementation of a proprietary application layer protocol on top of a MIL STD 188-184 DAMA Link Layer protocol. The application involves transfer of several military protocol messages (J-TIDS and TADIL-J) and NITFS formatted graphics files. Performed development and modifications to the Joint Stars RASP parallel processing DSP platform and the Joint Stars application software to enhance (double) the resolution of the Joint Stars synthetic aperture radar (SAR) imagery. Programming performed on DEC VMS systems and Joint Stars RASP parallel processing DSP platform (Mercury Raceway) using FORTRAN and C.

Computer Replacement Program *November 1997 – February 2000*

Developed system software and built-in-test (BIT) test software for the Joint Stars Computer Replacement Program's Radar Advanced Signal Processor (RASP). The RASP is the primary digital signal processing (DSP) component of the Joint Stars radar system. Most software developed for an embedded UNIX processor (SPARC) in a multiprocessor environment running on a VME/Raceway bus. Components programmed included the 1553B communications interface, a FDDI LAN interface, a GPS time source interface, a VME I/O card, Mercury Sharc processor cards, Mercury Power PC processor cards, and the Mercury Raceway Operating System.

AT&T Tridom Incorporated / GE Spacenet Incorporated
Senior Engineer, March 1996 – November 1997

Ported a real-time operating system (pSOS kernel) and proprietary communications software to a new platform. This Motorola 68040, VME based platform is for a satellite digital communications system. Code is in assembly and 'C'. Development carried out in a UNIX environment using Sun workstations. Trained in the VxWorks real-time operating system for future development projects.